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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,169	09/11/2003	Robert D. Nuckolls	P-9236	7593

24209 7590 02/02/2007

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EXAMINER	
PAN, DANIEL H	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,169	NUCKOLLS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-18 and 20-44* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/02/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Clams 1-44 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7,9-12,14,18,20-28, 30-34,36-37, 39-40,42 , 44 are rejected under 35 U.S.C. 102(b) as being anticipated by White (5,996,071).

3. As to claims 1,9, 15, newly amended features are also being treated in items b) and c) below in this action. White taught :

a) a branch prediction storage (see fig.6) including storage for branch direction indications (see the sets in way) and associable branch prediction qualifier indications (see v and history bits), wherein entries (or the branch prediction structure, claim15) provided for branch direction indications (256) are more numerous than those provided for branch prediction qualifier indications (see 128 entries in 252);

b) a branch direction indication (see the sets in way) indicates a direction (way) of a branch instruction instance (the branch instruction) with respect to branch prediction (predicted path , see col.17, lines 18-33) and the branch direction indication is associated with an instruction instance identifier (see v and history bits) that corresponds to said branch instruction instance (see predicted path depending on the history bits in col.17, lines 18-33); and

c) an outcome (taken or not taken) of the branch instruction instance is predicted based at least in part on the branch direction indication (see way) and a branch prediction qualifier (see v and history bits in fig.6C) associated with instruction instance identifier (see IP bits 0-4 in fig.6c).

4. Applicant only claims "a branch prediction storage" (see claim 1, line 2). No structure of the branch prediction storage has been recited into the claim. The examiner recited fig.6,b,c as the branch prediction storage. White's cache 204 and branch unit 250 (252) combined are a "branch prediction storage" because White taught the 204 cache in fig.6 b was the organization of an exemplary branch target cache as 4-way set associative, and the fig.6 c illustrated the entries in the branch target cache including for each entry the L1 cache entry index (the set number), byte location, and the way number for the cache line containing the target instruction in the L1 cache (see col.6, lines 64-67, col.7, line sl-6). Therefore, the L1 cache 204 branch target cache and 252 branch target cache are a branch prediction storage. Further evidence also shows that the 204 L1 target cache and 252 target cache are interconnected by delicate buses (see co1.11, lines 36-43).Therefore, L1 204 and 252 had dedicated connection and worked together as one prediction storage unit.

5. As to claim 25, White taught at least :

a) determining if an instruction instance is a branch instruction and if the instruction instance is represented in a branch prediction structure (see BTC) ;if the instruction instance is a branch instruction and is represented in the branch prediction structure, selecting in the branch prediction structure a branch direction indication

(history taken not take) that corresponds to an instruction instance identifier (see the identification tag) that corresponds with the instruction instance (see instruction pointer IP), and

b) selecting in the branch prediction structure a branch prediction qualifier indication that corresponds to the instruction instance identifier (see hit/miss entry selection in co1.18, lines 52-56); and performing branch prediction, wherein the outcome (predicted path see taken not taken in col.17, lines 18-46) based at least in part on the branch direction indication and the direction condition indication (see the update of the predicted result in col.20, lines 16-26);

c) the branch direction indication (predicted path taken or not taken) indicated a direction of the branch instruction with respect to branch prediction (see col.17, lines 18-46, see also col.3, lines 1-29 for the background teaching of using the BTC for predicted direction).

6. As to claim 2, 10, White also included some of the branch prediction qualifiers entries are associated with multiple ones of the branch direction entries (see the set number in fig.6c).

7. As to claims 3, 11, 18, White's branch direction indications and the branch prediction qualifier indications are accessible based at least in part on one or more of instruction instance identifiers and share addresses (see the tag address and NEXT IP).

8. As to claims 4,16, White branch prediction qualifier indications are accessible based at least in part on one or more of least significant bits of the instruction instance identifiers (see IP bits 0-4) and least significant bits of share addresses (see IP bits 5-11).

9. As to claims 5, 22,27, White also included program counters, physical addresses, and virtual addresses (see physical instruction pointers in co1.14, lines 42-44). No explicit virtual address was shown, but White taught virtual buffer (see co1.22, lines 13-14). Therefore, the virtual address must be included.

10. As to claims 6,12, 17, White also taught storage for one or more of branch history pattern indications and branch target instruction instance identifiers (see the history for pattern, see the tag for instance identifiers in fig.6c).

11. As to claim 7, White's branch direction indications (see set number in fig.6c) include one or more bits that indicate one or more of branch history, branch prediction, and branch pattern (see the history used for predicting taken and not taken in col.3, lines 10-22, see also the prediction BTC in lines 10-22, see also the prediction based on BTC in col.3, lines 1-9, see also fig.6c for BTC).

12. As to claim 14, see the history used for predicting taken and not taken based on BTC in col.3, lines 1-9, see also fig.6[c]);

13. As to claim 20, White also taught one or more history pattern and instruction instant identifier (see the tags and the history fields in fig.6c).

14. As to claim 21, White also included branch direction indications (see taken not taken in co1.3, lines 10-22, see also the prediction based on BTC in co1.3, lines 1-9, see also fig.6c for BTC)

15. As to claim 23, White also included branch prediction in part on the determined branch direction indication (taken, not taken) and the determined branch prediction qualifier indication (see valid bit).

16. As to claim 24,28, White also updated the branch prediction qualifier indication and the branch direction indication with respect to outcome of the instruction instance that corresponds to the instruction instance identifier (see the storing the indices into the entries of BTC in co1.18, lines 39-44).

17. As to claim 26, White also included at least in part one or more least significant bits (see co1.18, lines 38-56).

18. As to claim 30, White taught at least :

a) means for sharing branch prediction qualifier indications (see history, V in fig.6c) between multiple branch direction indications (see set number, and tag, see also prefect and storing for fetch and updating in co1.17, lines 18-39, co1.18, lines 25-38. See also decode for predicted paths of branch in co1.14, lines 25-41).

b) a branch direction indication (see the sets in way) indicates a direction (way) of a branch instruction instance (the branch instruction) with respect to branch prediction (predicted path , see col.17, lines 18-33) and the branch direction indication is associated with an instruction instance identifier (see v and history bits) that

corresponds to said branch instruction instance (see predicted path depending on the history bits in col.17, lines 18-33); and

c) an outcome (taken or not taken) of the branch instruction instance is predicted based at least in part on the branch direction indication (see way) and a branch prediction qualifier (see v and history bits in fig.6C) associated with instruction instance identifier (see IP bits 0-4 in fig.6c).

19. As to claims 31,32, see also prefect and storing for fetch and updating in co1.17, lines 18-39, co1.18, lines 25-38. See also decode for predicted paths of branch in co1.14, lines 25-41).

20. As to claims 33, 44, White taught at least :

a) branch direction entries (see fig.6c) accessible by first representations (tag) that correspond to branch instruction instance identifiers (instruction pointer) ; and

branch prediction qualifier entries (see history, valid bit) accessible by second representations (see set number) that correspond to the first representations, wherein the branch prediction qualifier entries (128)are fewer than the branch direction entries (256);

b) an outcome (taken or not taken) of the branch instruction instance is predicted based at least in part on the branch direction indication (see way) and a branch prediction qualifier (see v and history bits in fig.6C) associated with instruction instance identifier (see IP bits 0-4 in fig.6c, see also the predicted taken and not taken path in col.1, lines 1-36, see also the predicted taken and not taken path in col.17, lines 11-39).

21. As to claim 34, White included leas significant bits (see the least significant bits 11:4).

22. As to claim 36, White also included more history entries (see 128 entries in fig.6c).

23. As to claim 39, White also included a processing system comprising :

a) branch prediction storage having entries (see fig.6a [252], see figs. b,c for details) for branch direction indications (see set number) and entries for branch prediction qualifier indications (see valid bit), wherein the branch prediction storage has more branch direction entries (256) than branch prediction qualifier entries (128) ;

b) a branch direction indication (see the sets in way) indicates a direction (way) of a branch instruction instance (the branch instruction) with respect to branch prediction (predicted path , see col.17, lines 18-33) and the branch direction indication is associated with an instruction instance identifier (see v and history bits) that corresponds to said branch instruction instance (see predicted path depending on the history bits in col.17, lines 18-33); and

c) an outcome (taken or not taken) of the branch instruction instance is predicted based at least in part on the branch direction indication (see way) and a branch prediction qualifier (see v and history bits in fig.6C) associated with instruction instance identifier (see IP bits 0-4 in fig.6c).

d) a bus coupled to the processor(see fig.1 processor and bus) and

e) memory coupled to the bus (see the memory in fig.1).

24. As to claim 40, the branch direction entries are accessible with values that correspond to instruction instance identifiers (see IP) and the branch prediction qualifier entries are accessible with least significant bits of those values (see 11:5).

25. As to claim 42, White also included the values result from one or more operations performed on the instruction instance identifiers (see the valid and history fields in fig.6c).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 8, 13, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (5,996,071) in view of Jain et al. (5,553, 255).

27. As to claims 8, 13, 29, limitations of parent claims already discussed above. White also included a valid bit (see V in fig.6c). However, White did not specifically teach strength and the confidence of the branch direction. White taught branch taken and not taken in the BTC (see col.3, lines 10-22, see also the prediction based on BTC in co1.3, lines 1-9, see also fig.6c for BTC). The taken and not taken could be read as a confidence. However, the strength of the branch taken is not being taught. Nevertheless, Jain taught a branch prediction system including the strength of branch prediction (see strongly taken in col.7, lines 28-55). It would have been obvious to one

of ordinary skill in the art to use Jain in White for including the strength of the branch prediction as claimed because the use of Jain could provide White the ability to predict the branch directions on additional criteria of the predictions ,such as the level of the predicted taken branches, and because White also taught indications of the predicted taken and not taken with actual taken and actual not taken (see fig.10), and since predicted taken might end up actual not taken, which was a suggestion of the need for inculcating additional parameters such as the level or strength of the predictions into the system in order to enhanced the efficiency of the prediction results, and for doing so, provided a motivation.

28. Claims 35,41 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (5,996,071) in view of Smith (4,370,711).

29. As to claims 35,41, limitations of parent claims already discussed above. White did not specifically show hashed address as claimed. However, Smith taught a hashed address (see col.& lines 10-25). It would have bee obvious to one of ordinary skill in the art to use Smith in White for including the hashed address as claimed because the use of Smith could provide White the ability to integrate the branch address into a predefined format with reduced number of bits, therefore, minimizing the hardware overheads, and White did disclosed the use of partial bit for branch address (see the tag), which was a suggestion of the need for using smaller number of address bits, such as a hash, in order to minimize the circuit space, for doing so, provided a motivation.

30. Claim 38, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (5,996,071) in view of Chang (5,687,360).

31. As to claims 38, 43, limitations of parent claims have been discussed above. White did not specifically show the shift register for the branch history as claimed. However, Chang disclosed a shift register for a branch history (co1.4, lines 38-45). It would have been obvious to one of ordinary skill in the art to use Chang in White for including shift register as claimed because the use of Chang could provide White to save the branch history data in a predetermined order, and it could be achieved by reconfiguring the shift register of Chang into White with modified control parameters (e.g. the width of the shift register, the R/W port), such as the shift register of Chang could be recognized by White, and because White did taught a shift of his branch information into the buffer, and therefore, provided a suggestion for using a shift register in order to provide predefined set of sequence.

32. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the at least some of the least significant bits of the value are unchanged from the instruction instance identifier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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